RISC-V Arrives

Yunsup Lee, CTO at SiFive, is on a mission to disrupt chip design. "We're trying to change the chip design experience into something like ordering pizza online," he told the audience in his keynote presentation at the Embedded Linux Conference & Open IoT Summit last month in Portland, Oregon.

In SiFive's pizzeria-esque vision, a customer visits a website and begins a template driven process not unlike standing up a virtual environment in the cloud. First, select from a basic offering of processor cores complete with standard peripherals already onboard. Next, stop at the marketplace and grab some third-party components. Finally, top it all off with your own value-added custom IP. Toss the whole thing in the oven and, voila, a billion custom chips roll off the line.

At the heart of this process are RISC-V processor cores. RISC-V, the open source ISA out of U.C. Berkeley, has been on something of a tear lately. The RISC-V Foundation roster has grown to over 100 members, including major tech drivers like Google, NVIDIA, Qualcomm and Samsung. RISC-V pioneer David Patterson (along with his colleague John Hennessy) was recently recognized by the Association for Computing Machinery with its prestigious A.M. Turing Award for his contributions to computer architecture design.

The RISC-V project began at Berkeley in 2010 and the team made its first public push at the 2014 HotChips Conference. However, 2017 was the year the fledgling ISA seems to have captured the tech world's collective awareness. More than 500 people attended the November 2017 RISC-V Foundation Workshop, two days of presentations and demos in Milpitas, California. Headlines for RISC-V initiatives have become standard fare, not only in the trade pubs but in general business and news outlets as well.

Among the larger Foundation members with migrations to RISC-V underway are NVIDIA and Western Digital. NVIDIA is basing its next-generation FALCON controllers on RISC-V. FALCONs are embedded across a range of NVIDIA chips as the control engine for its GPUs. Current generation FALCONs are a proprietary RISC architecture. After 10 years of deployments, the limitations of the FALCON legacy architecture are bumping up against increasingly complex use cases which demand threading and large virtual memory spaces. After reportedly evaluating virtually every available solution, NVIDIA chose RISC-V for the path forward.

For its part, storage giant Western Digital is planning to migrate its existing product line to the RISC-V ISA and will be using it in all future products. The company will be using a mix of internally designed and third-party processors and plans to be shipping out more than a billion RISC-V cores a year. Like NVIDIA, Western Digital's use cases are becoming increasingly complex and its HDD and SSD offerings need increasingly robust multi-core processors to handle general management, signal processing, and error

correction. At the same time, the company is working to position itself as a provider of Big Data and Fast Data solutions. It wants to develop increasingly powerful products that move processing closer to the data and execute analytics in real time.

It's no surprise that SiFive, which tags itself as "the first fabless provider of customized, open-source-enabled semiconductors," figures prominently in the RISC-V movement. Its three founders, Krste Asanovic, Andrew Waterman, and Yunsup Lee were fundamental in the development of the instruction set. Asanovic is a professor at Berkeley and leads the RISC-V project there, while Waterman and Lee are credited as co-developers of the ISA.

Since forming in 2015, SiFive has been busily assembling a network of companies to offer low or no-cost IP for proof of concept projects as part of its DesignShare ecosystem. Think Silicon, for example, makes its ultra-low power GPU technology available at a reduced cost. Other DesignShare offerings include USB solutions from Corgine and embedded non-volatile memory from eMemory. The startup has now received a $50-million funding injection to build out its cloud service design platform and plans to be live later this year.

SiFive has also been pushing out actual proof of concept silicon. Its Freedom E310 microcontroller grabbed headlines in November 2016 as the first commercially available RISC-V processor. You can buy them in packs of five, or on an Arduino form-factor development board called the HiFive1. Coming soon is the HiFive Unleashed development board, hosting the Freedom U540, a Linux-capable, multi-core, RISC-V processor.

Beyond the higher profile projects like those from NVIDIA, Western Digital and SiFive, RISC-V has been steadily entrenching itself across the design cycle. A growing list of IP vendors, including Andes Technology and Codasip, have RISC-V cores ready to be implemented in silicon, while Microsemi and others offer softcores that run on FPGAs. Multiple flavors of Linux are available, with RISC-V support for binutils, gcc, newlib, glibc and more. Lauterbach has implemented support for SiFive's processors in its TRACE32 toolset. IAR Systems, citing "an increasing demand from our customers" is targeting a 2019 release of RISC-V support through its IAR Embedded Workbench toolchain.

A year ago, or maybe two, it might have been easy to pass over RISC-V as an academic project with little real-world relevance. No longer. While some industry analysts caution that there is still a long road with lots of remaining work ahead, the question of the day is not whether RISC-V will take its place alongside the likes of ARM and x86, but rather how thoroughly the ISA will shake-up the processor market.

There's good reason to believe that the shake-up will be fairly thorough. Core tenets of the RISC-V value proposition include the notions that (1) the art of instruction set design has matured with diminishing returns from minor differentiation, and (2) industry players have more to gain leveraging a common ISA with proven implementations and robust tools, than they do pursuing custom designs for which they must do all the heavy lifting themselves. From embedded controllers to multi-core server processors, every successful RISC-V implementation strengthens that underlying value proposition. As vendors continue to face increasing complexity demands coupled with increasing design costs, it appears that an open ISA is an idea whose time has come.